REMARKS

Reconsideration of this application is requested. Claims 18, 20, 23, 31, 33, 41 and 45 to 49 are pending. The pending independent claims are 18 and 49.

The objection to the drawings have been overcome by amending claim 18 to make more clear that the source enable signal output circuit is included in the power source control circuit. No changes to the drawings are necessary.

The rejection of claims 18, 20, 23, 31, 33, 41 and 45 to 48 under section 112, first paragraph, for lacking an enabling disclosure is traversed. As suggested in the Action, the claims have been amended to use the term "power source control circuit" which is the same term used in Figure 25 and the application as originally filed. Further the claims have been amended to delete term "means for" to avoid any suggestion that the claims use "means plus function" limitations.

The application as filed discloses and provides an enabling disclosure of "a panel power maintaining means" and "a source enable signal output circuit for outputting, to the source driver control circuit, a source enable signal." These terms refer to the "power source control circuit" which is shown in the Figures at reference number 56, and are described in full and in detail in the original application at, for example, pages 40 and 45. To avoid any confusion in claim 18, the term "power source control circuit" has been substantial for "a panel power maintaining means", and the claim has been amended to

state that the power source control circuit includes the "source enable signal output circuit".

The application as filed discloses and provides an enabling disclosure for the limitation that "said source driver control circuit which, in response to the source enable signal causes said source driver to apply an OFF voltage to said pixel electrode to turn OFF a liquid crystal" of claim 18. The amendment of claim 18 should also resolve the 112 rejection of dependent claim 23.

The rejection of independent claim 49 as being anticipated by Yasui et al (U.S. Patent No. 5,248,963 – Yasui) is traversed.

Claim 49 recites signals formed of "rectangular wave signals" being applied by the LCD erasing circuit. The claim further requires that the that the erasing circuit "applies rectangular wave signals, identical in terms of phase and potential, respectively into said pixel electrode and said opposing electrode during the certain period" which follows the power source being turned off.

Yasui does not disclose the rectangular wave signals, that are identical in terms of phase and potential, respectively into said pixel electrode and the opposing electrode. Yasui states that during a certain time period (T) (which occurs after the power source is turned OFF) a constant common potential (EG or E_2) is supplied to the display electrode 12a and the opposing electrode 12b. Yasui fails to disclose applying rectangular wave signals that are identical in terms of phase and potential are supplied to the display electrode and the opposing electrode.

Yasui discloses applying a constant common potentials (E_2 and then EG) to clear the pixels of a display. These potentials are applied sequentially and are not applied cyclically as a rectangular wave. A clear signal is applied to begin powering down a display and to commence period T. During period T the power supply is turned off and the charges in the pixels are allowed to discharge. Yasui col. 6, lns. 1-11. During period T, the E_2 voltage level is first applied to common counter pixel electrode 12b. Yasui, col. 3, lns. 58 to col. 4, ln. 2 and col. 6, lines 3 to 6. Yasui discloses in column 6, lines 3 to 6 that a common potential is supplied to a display electrode 12a and an opposing electrode 12b (a DC voltage E_2 is supplied to the opposing voltage 12b) within a time (T) after the power is turned OFF.

During the period T, the voltage E_2 discharges to ground. Yasui (column 5, lines 4-6) states that "[t]he supply of these voltages V_1, V_2, V_3, E_1, E_2 and E_3 is stopped when the power supply of the display device main body is turned OFF." Yasui teaches that a ground potential EG is supplied to both the display electrode 12a and the counter electrode 12b within the time T after the power is turned OFF. Yasui (column 5, line 6, to column 6, line 1) describes that "[t]he source bus driver 16b is arranged so that the potential as its output terminal goes to the common potential EG at substantially the same time as the operating voltages E_1, E_2 and E_3 drop to the common potential". There is no teaching of cyclically applying EG and E_2 voltages in a rectangular wave fashion to the source bus for the pixels.

The Action incorrectly characterizes Yasui as disclosing at column 6, lns. 1-11 (see also column 3, line 58 to column 4, line 16), that a DC voltage (E_2 and common) is supplied to the display electrodes 12a and 12b by the source buses 14t through 14_l through 14_n to clear the display. Yasui (column 1, lines 45 to 60) states that the E_2 is a DC voltage. This description in Yasui indicates that a DC voltage is supplied to both the display electrode 12a and the counter electrode 12b within the time T after the power is turned OFF.

The rejection of claims 18, 20, 23, 41 and 45 to 48 as being anticipated by Yasui et al (US Patent 5,248,963 -- Yasui) in view of Tsuboyama et al (US Patent 5,592,191 – Tsuboyama) is traversed.

Independent claim 18 recites several elements that are not disclosed or suggested by Yasui and Tsuboyama including:

- Claim 18 recites a "source driver", a "source driver control circuit", and a "source enable signal output circuit". These circuit elements are not disclosed in Yasui in the manner recited in claim 18.
- Applying an OFF voltage as a video signal during the "certain period" to erase the pixels of the LCD.
- The source enable signal causes the source driver control circuit, to command the power maintaining means to apply an OFF voltage to the pixel electrodes.

- The source driver control circuit does cause the OFF voltages to be applied to the pixel electrodes.

A "source enable signal" that is "at a selecting level during the certain period [which is a period following power being turned off, and the selecting level] is inputted into said source driver circuit so that said pixel electrode and said opposing electrode receive an OFF voltage that turns OFF a liquid crystal." *See, e.g.*, Appln. pp. 39-49 (emphasis applied).

Yasui discloses a method to erase a liquid crystal display in which the source bus and gate bus driving circuits connected to the source and gate of thin-film-transistors (TFT 13) maintain the TFTs at an active level for a predetermined period after turning OFF the power source. Keeping all pixels active after the power is turned off discharges accumulated charges in the pixel capacitance in a short period. Yasui, col. 6, lns. 33-42. Yasui teaches that after the power supply is turned OFF, each pair of display and counter pixel electrodes are grounded, i.e., discharged to a common potential, within a time period (T) by discharging both electrodes. *See* Yasui col. 6, lns. 3-9.

Yasui discloses supplying a common potential to both a display electrode 12a and a counter electrode 12b within a time (T) after the power is turned OFF (see column 6, lines 3 to 6). Yasui discloses that pixel data (D) is set to a logic "0" to clear the display. Yasui, col. 3, lns. 59-61. The pixel data is loaded into a shift register and then applied to the pixels. Yasui does not disclose a feature in which "source enable signal output

circuit" generates a "source enable signal" that is inputted to the source driver control circuit during a predetermined period after the power source is turned OFF.

The Action mischaracterizes Yasui with respect to the power holding circuit 22 and power circuit 23 which apply a post-OFF voltage to the gate bus drive circuit 17, rather than the source bus drive circuit 16. *See* Yasui, col. 4, lns. 59-64. Contrary to the Action, the power holding circuit 22 and power circuit 23 and associated capacitor 25 and inverter 27 (not identified in drawings) relate to the gate bus drive circuit 17 and not to the source bus drive circuit 16. The Action states that a capacitor (25), a resistor (26), an inverter (27), and a voltage V_B correspond to the source driver control circuit, and the source enable signal respectively. However, Yasui Fig. 5 and the descriptions in column 5, lines 8 to 53, make clear that these elements are provided for supplying a voltage V_{CL} to a gate bus driver circuit 17, and have nothing to do with a source bus driver circuit 16. Yasui teaches that a post-OFF signal high-level output voltage (V_{CL}) is applied to cause the gate bus driver 17. Yasui, col. 5, lns. 31-64). The V_{CL} high-level output voltage causes the TFTs for each pixel to be turned ON such that the source bus driver 16b to apply a common potential to the display electrodes. Yasui, col. 5, ln. 59 to col. 6, ln. 11.

The source of the source control signals (D, PCK, and M) for the source bus drive circuit is not disclosed in Yasui. Even assuming that there must be a signal source for supplying to source bus circuit 16 the D, PCK and M signals, Yasui does not disclose a source enable signal output circuit for supplying a source enable signal to a source driver

control circuit to cause the source driver to have an OFF voltage applied to the pixel electrodes.

Unlike Yasui, claim 18 herein recites that a source enable signal is inputted to the "source" driver control circuit at a "selection level" during the predetermined period after the power source is turned OFF. Such use of the "source" enable signal does not complicate the circuit arrangement and allows application to the pixel electrode and the opposing electrode, a voltage for turning OFF the liquid crystal. Because Yasui teaches display erasing by means, (e.g., gate control and loading "O" into source driver) other than a source enable signal, it teaches away from the invention recited in claim 18

Tsuboyama does not relate to active element displays, such as are recited in the claims of this application. Tsuboyama primarily discloses a ferroelectric liquid crystal display having a memory function, in which a non-zero voltage is applied to erase the contents of the picture elements of the display. Tsuboyama, col. 1, lns. 9-12 ("The present invention relates to . . . display devices having a memory effect, such as ferroelectric liquid crystal panels."). The "memory effect" described in Tsuboyama relates to irregular orientation of the liquid crystals in ferroelectric LCD display that are caused by a DC voltage applied to the display. Tsuboyama, col. 1, lns. 33-51. The irregular orientation of liquid crystals that is the subject of Tsuboyama is unrelated to the problem of residually charged pixels in an active matrix display, that is the subject of the present invention.

The display state in Tsuboyama's display is maintained after the erasing voltage has been applied is because Tsuboyama's display device is a ferroelectric liquid crystal display having a memory property. As clearly shown by Fig. 5(A) of Tsuboyama, the voltage (potential difference) to be applied after the TE period is 0. No switching occurs during a bistable state after the TE period so that the display state is maintained.

With respect to Tsuboyama, the Action asserts that the data side Vc control signal in Figure 5A is equivalent to the source enable signal recited in claim 18 that is at a selecting level during the erase period TE. however, as the name implies, the data side Vc control signal of Tsuboyama in Figure 5A is a control signal which controls Vc application to the data liens. The data side Vc control signal in Figure 5A is at selecting level during a period in which Vc is being applied to the data lines, that is, non-erase periods TVc1 and TVc2. The data side Vc control signal in Tsuboyama Figure 5A is at selecting level during the erase period Te. Figure 5A shows that the data side Vc control signal is HIGH only during the periods TVc1 and TVc2 and LOW during the erase period TE. In contrast, claim 18 uses a source enable signal which is at selecting level during a certain period in which the liquid crystal is turned off. This source enable signal is neither disclosed nor suggested by Tsuboyama.

These problems and solutions are associated with the pixel switching elements of active matrix displays, and are foreign to ferroelectric liquid crystal displays, as is disclosed in disclosed in Tsuboyama, that have no corresponding switching element. With Tsuboyama's ferroelectric liquid crystal, once the voltage is applied to the liquid

crystal for shifting to a stable state, this display state is maintained. A reset pulse (erasing voltage) is applied to erase the display, and without a distinction as to whether the ON-level signal or the OFF-level signal is applied, a voltage (erasing voltage) is returned to the initial state, and the state is maintained because of a memory property of the liquid crystal. Accordingly, Tsuboyama does not disclose that the response speed can be increased, which is one of the features of the present invention.

Tsuboyama discloses a simple matrix, liquid crystal display in which scanned data lines apply voltages of different polarity to change the alignment of liquid crystals in a pixel of a display. Tsuboyama, col. 1, lns. 14-31. To clear a display, Tsuboyama teaches that the following five steps are to occur sequentially in a simple matrix, liquid crystal display having a ferroelectric liquid crystal layer:

(1) A logic circuit 107 receives a detection signal indicating that the power supply has been turned OFF or otherwise interrupted (Tsuboyama, col. 3, lns. 26-29; col. 4, lns. 42-43).

(2) A voltage V_C is applied to all scan and data lines in the display (indicated as TV_{C1} in Figs. 5A and 5C of Tsuboyama). Tsuboyama, col. 4, lns. 38-43.

(3) A negative voltage (V_4) is next supplied to all scan and data lines in the display (indicated as TE in Figs. 5A and 5C of Tsuboyama). Tsuboyama, col. 4, lns. 43-52.

(4) A voltage V_C is next applied to all scan and data lines (indicated as TV_{C2} in Figs. 5A and 5C of Tsuboyama). Tsuboyama, col. 4, lns. 52-55.

(5) Finally, all of the scan and data lines are grounded. Tsuboyama, col. 4, lns. 55-60.

According to Tsuboyama et al. (as shown in Figs. 5A to 5C) in steps (2), (4) and (5) the same voltage is applied to both scan and data lines, such that there is no polarity difference applied to activate the pixels.

Because Tsuboyama does not disclose an active matrix having pixel transistors or other pixel switching elements, it is improper to view Tsuboyama as switching pixels ON and OFF as is done in the present invention. What Tsuboyama et al do teach is that a voltage difference (negative V_4 and zero voltage V_c) is applied across a ferroelectric display to erase the display. This voltage difference changes the orientation of liquid crystals in the display. Accordingly, there are no pixels that are turned ON and OFF in the display disclosed in Tsuboyama.

All claims are in good condition for allowance. If any small matter remains outstanding, the Examiner is requested to telephone the undersigned. Prompt reconsideration and allowance of this application is requested.

Respectfully submitted,

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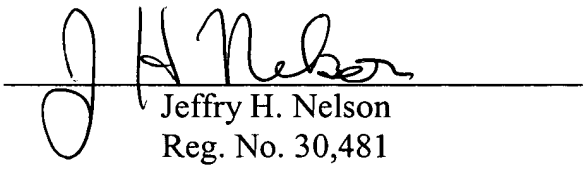
By: 
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